Comparison of Diode vs. Synchronous Rectifier Used in Dual Half Bridge DC-DC Converter with Reduced Circulating Current

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Abstract. Each electronic device, from any consumer or industrial sector needs power supply. This power supply must satisfy nowadays certifications and efficiency standards. One of the progressive topology shall be dual half-bridge topology. This topology is formed by two branches – lagging and leading.

In this paper, the efficiency of dual half bridge converter is analyzed. For this purpose experimental prototype with diode rectifier as well as synchronous rectifier is evaluated. The concept of proposed converter is targeting efficiency higher than 96%.

Keywords
Zero circulating current, dc-dc converter, half-bridge, dual converter

1. Introduction

The most popular topology for high-power and high-density power supply is phase-shifted, full-bridge dc-dc converter. It is mainly for its wide use, and its capability to achieve zero-voltage switching (ZVS) for wide operation region. ZVS mode is commutation mode, which minimizes switching losses, and thus gives rise to efficiency of converter.

A big lack of this topology is circulating current, whose highest impact is evident mainly during heavy load of the converter. At light loads the circulating current is minimal, but on the other side, loss of ZVS conditions is present. Elimination of circulating current enables design of converter to be smaller, and contributes to a higher efficiency of converter. This can be performed by topology of dual H-bridge, whose construction reduces circulating current to minimum. Compared to full-bridge converter, we can consider this current to be zero. Low power losses bring another advantage. Demand for a heat sink is smaller, because of lower power losses, which convert into a heat.[1-2]

2. Converter Operation

The converter's two half-bridge inverters always operate at a 50% duty cycle. When one of the switches of half-bridge is turned off, the magnetizing current and reflected output current discharge and charge parasitic capacitances of switching components. The waveforms of main variables during the steady-state operation of the converter are shown in Fig. 2.

Fig. 1 Dual-half bridge DC-DC converter
Interval 2 with $t_2 \leq t \leq t_3$

At time $t_2$, transistor $Q_1$ is turned off. Capacitor $C_{Q1}$ is charged up by reflective current $I_{L2}$. The voltage across transformer $T_2$ reverses polarity opposite to interval 1. Diode $D_4$ conducts and takes current from $D_6$. $T_2$’s magnetizing current charges capacity $C_{Q1}$ and discharges $C_{Q3}$. Diode $D_5$ starts conduct together with diode $D_3$, and both inverters share output current $I_{L1}$.

Interval 3 with $t_3 \leq t \leq t_4$

At this interval, the inverters share output current. Because the voltages $V_{M1}$ and $V_{M2}$ are the same, the current shift from leading inverter to lagging inverter is slow. $I_{L2}$ is still decreasing, what is reflected as output voltage drop. Increase of the current $I_{L1}$ compensates output voltage drop, and minimizes output ripple voltage.

Interval 4 with $t_4 \leq t \leq t_5$

At $t_4$, $Q_1$ is turned off and $C_{Q1}$ is being discharged. Diode $D_3$ is open, while current $I_{L1}$ falls to the value of magnetizing current. During this time $C_{Q2}$ is fully discharged and at $t_5$ switch $Q_2$ is able to turn on at zero voltage conditions. Diodes $D_4$ and $D_8$ are shorted by $T_1$’s secondary current, what is the reason that energy from $T_1$ does not contribute to discharge capacitance $C_{Q2}$. Resonant inductor resonates with capacitances $C_{Q1}$ and $C_{Q2}$. With the use of proper value of deadtime, $Q_2$ can be turned on at ZVS conditions.

Interval 5 with $t_5 \leq t \leq t_6$

At $t_5$, $Q_2$ is turned on and resonant current $I_{L2}$ decreases quickly. After it this current starts to build up in the opposite direction. When reflected resonant current is higher than output current $I_{L1}$ and $D_8$’s reverse-recovery current, $D_8$ stops conducting at $t_6$. Time $t_6$ is the end of one half-cycle of converter operation.

3. Application with synchronous rectifier (SyncFET)

For this type of converter it is also possible to utilize synchronous rectification at the secondary output stage. In standard topology (fig. 1), the transformers’ $T_1$ and $T_2$ secondaries are connected to the ground. This configuration can be utilized, when diode rectifier is considered. But such configuration for synchronous rectification could cause some problems, when SyncFET drivers are used. Main problem which is eliminated when common source connection is used is driving of high-side transistors. If common source connection won’t be used, then drivers with isolated outputs must be used. This solution is very expensive and not preferred.

4. Experimental results

A 2-kW, 400-V/48-V, DC/DC converter was designed for experimental measurement of basic steady-state behavior and for verification of proposed converter operation. Our primary goal was development of DC/DC
converter with high efficiency and high power density, which would be used as power-supply for telecom-server application.

Based on the results from detailed simulation model we determined the power transformer turns ratio to $n=3$. Magnetizing inductance of transformer can have variable value from 600μH to 1100μH for our application. After proper calculation with selected magnetic core PQ35/35 we determine the value of magnetizing inductance to 900μH. The number of primary turns was calculated as follows:

$$N_1 = \sqrt{\frac{L_1}{A_1}} = \sqrt{\frac{900 \times 10^{-6}}{4700 \times 10^{-9}}} = 13,838 \div 15 \rightarrow N_2 = 5 \quad (3)$$

For 15 turns of transformer’s primary, the value of magnetizing inductance is:

$$L_{T1} = A_1, N_1^2 = 4700 \times 10^{-9}, 15^2 = 1,058 \, mH \quad (4)$$

Resonant inductor resonates with parasitic capacitances $C_{Q1}$ and $C_{Q2}$. $C_{Q2}$ can be fully discharged when next formula for the value of resonant inductor is valid:

$$L_r = 16 \times f_s^2 \times L_{T1}^2 \times (C_{Q1} + C_{Q2}) \quad (5)$$

After determination of switching frequency ($f_s$), T1’s magnetizing induction ($L_{T1}$) and parasitic capacitance ($C_{Q1}$ and $C_{Q2}$) we can calculate resonant inductor, where $L_r = 20 \, \mu H$.

Minimal drain-source voltage of switches Q1-Q4 is:

$$U_{Qmin} = 1.1 \times U_{INmax} = 1.1 \times 1,420 = 462V \quad (6)$$

Minimal diode’s blocking voltage is:

$$U_{Dmin} = 1.1 \times 2 \times \frac{U_{INmax}}{n} = 2.2 \times \frac{210}{3} = 154V \quad (7)$$

Proposed converter can be embedded to rack shelf format U1. The physical hardware is shown at Fig. 3. On the left side, the primary part of converter is being located, while in the center of converter the power transformers and signal’s optocoupler are being placed. On the right side, diode or synchronous rectifier together with output inductors, output capacitors and hall effect-based linear current sensor are placed.[5]

The circuit parameters and components used during this test were:

- Primary MOSFETs: STW55NM60ND
- Secondary MOSFETs: IPP110N20N3
- Secondary diodes: STPS60SM200C
- Magnetizing inductance: 1030μH
- Output inductor: 28μH
- DC blocking capacitors:
  - Resonant inductor: 20μH
- Transformer turns ratio: 15:5:5
- Output capacitor: 3x820μH

All the measurements were undergone at phase-shifted control mode. This is the reason, why better performance of converter was not achieved during low-power load. However, we achieved expected results. With the diode-based output rectification, the converter operates at max. 97% of efficiency. In the case of synchronous rectification with SyncFETs, the efficiency was improved by at least 0.5%.

When converter operates at full load, we can see difference in the shape and amplitude of diode SyncFET current. First difference is turn – on value of this current. SyncFET has little bit lower value of turn-on current, whereby after it, sharp rise of this current can be visible. This is caused due to conduction modulation and development of conduction channel of transistor structure. This process is much faster compared to diode, because the resistance of the on-state of SyncFET is lower compared to diode. In this case, the phase-shift is the same at both versions of rectifier. Diode rectifier has steeper falling edge than reverse diode in SyncFET, because Schottky diode has shorter recovery time.[4-5]

The performance comparison from the efficiency point of view, between diode rectifier and SyncFET rectifier is shown on Fig. 6. It can be visible, that synchronous rectifier is showing better performance in the whole range of operating region, whereby difference is above 0.5%.
Here it must be said, that further improvement can be
done, when PWM together with PSM during light load will
be used. Also, better performance of utilization of
synchronous rectifier will be evident, when higher currents,
will flow through the output stage of converter (> 50A).
[4-5]