A Differential Fully Integrated UWB Radar

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Abstract. The main scope of this article is to introduce embedded UWB radar as a monolithic integrated structure. Results of the entire system integration into the one monolithic structure are presented. Integrated structure is composed of one transmitter and one wide-band receiver operates in full differential mode. Newly improved building blocks of the transmitter were used. For better controlling of this system, a low voltage differential control signals LVDS interface was added to improve the synchronization in the case of the cooperative UWB sensing. This integrated structure in 0.35 \( \mu \)m SiGe BiCMOS technology was manufactured. The power consumption of this system is 0.4 W and the operating frequency range is across the UWB band from 200 MHz to 9 GHz. The power of the generated stimulus signal is up to 1 mW, which is enough for the non-invasive remote sensing purposes. UWB devices like this operate by continuously emitting electromagnetic wave mode.

Keywords

UWB radar, PRBS sequence, Integrated Circuit, ASIC.

1. Introduction

Under the term UWB radar, a sophisticated and powerful device for non-destructive remote sensing can imagine. Devices like this, are mostly used for the longtime remote sensing as a single device or connected into the cooperative sensor networks with the centralized structure. Before the start of the measuring with this UWB radar, some significant parameters have to be set. We need to know at least dimensions of the measured area, the distance between used antennas, parameters of the used UWB radar and good power source as well. Therefore, if measurements are taken somewhere in the exterior conditions, the setting of the measurement may take a lot of effort and time. This paper presents a solution that supposes to use smart hand-held UWB device that can be driven by the batteries or solar panels. Presented integrated UWB radar as a solution that can decrease power consumption and use the frequency spectrum more efficiently is introduced. Several past periods we were focused on the problem of integrating the whole UWB radar system into the small integrated form. It was very challenging and fruitful process from the idea, system integration, and final results. Solving problems of system integration, impedance matching, power consumption, efficient use of space on the chip and many others until to desired results. The main scope of this paper is a brief overview of our concept of UWB radar integrated into the monolithic system on a chip (SoC) structure. In the next section, a theoretical background about monolithic circuits and related work is discussed. Section III describes of used monolithic structure and its design. Section IV deals with testing and measurements of the proposed SoC solution. Finally, pros and cons of our experimental results are summarized in the conclusion.

2. Theoretical background

Integrated monolithic SoC systems are still very often mentioned issues in many scientific articles. For hardware engineers, it is one of the most arduous hardware challenge. Progressive new methods of the integrating the entire system into one monolithic structure are still developed. The frequency range of this UWB device is very high (see section IV). If used frequency arises up to higher level, some of the discontinuities can appear. In the area of analog circuits or mixed signal integrated structures [1], they are often influenced by the effect of noise, obstruction or delay [2], [3]. Generated stimulus signal, pseudo-random binary sequence (PRBS) signal has a significant signal swing. In the process of generating a stimulus signal, switching noise also arises. In the article [4] a switching noise reduction techniques by using the balanced current steering topology methods are discussed. These methods are based on using a differential circuit wherever it is possible. Presented monolithic UWB radar is fully differential structure. Source of the clock signal includes differential amplifier designed as a BalUn buffers, transmitter and receiver and all of the used blocks are differential (see. Fig1). Differential structures are more stable, more resistant to the oscillations and offers lower susceptibility to the interference. All of the input and output ports as a differential pair are routed out. Intermodulation distortion, especially at higher frequencies, can be eliminated considerably as well.
3. Monolithic Structure of UWB Radar

Our concept of the monolithic integrated UWB structure consists of two main stages, transmitter and receiver (see Fig.1). All of the transmitter and receiver sub-circuits in the mixed signal architecture were manufactured as an application specific integrated circuit (ASIC). Actually, antennas as another main part of the proper functionality are needed. In our case, antennas as an external parts of the UWB radar were used. However, in concept of the monolithic SoC systems a new method of the integrated antennas can be investigated. Interesting way is to use an integrated high band antenna (ILA) [5]. Integrated SoC structures with ILA antennas can be easily integrated into the package with using the standard assembly process.

3.1. Design of the Monolithic Structure

The overall structure of the proposed SoC as a simplified block diagram is shown in Fig.1. The concept of these structures is derived from the conventional UWB devices and is supplemented by the LVDS interface. Further, the structure comprises the synchronization unit and input buffer, but the more detailed description of this blocks exceeds the scope of this article. Switching noise reduction by balanced current steering topology and another techniques with using a shielding rings and barriers have been used for testing.

![Fig. 1. Simplified block schematic of the SoC structure](image)

3.2. Used manufacturing process

The structure of the transmitter, receiver, and synchronization unit is largely characterized by the mixed analog and digital circuits. It can be imagined as a usage of the two types of transistors. CMOS transistors for the digital part and heterojunction bipolar transistors (HBT) for the analog part. For this reason, the proper semiconductor technology was necessary to choose. The company called Austriamicrosystems (AMS) [6] provide good solutions, that offers the production of ASIC circuits. Especially it is a multi-project wafer (MPW) manufacturing process or pool service which was used in our case. Chosen technology from AMS is called 0.35 μm SiGe BiCMOS or S35D4 technology. This technology has very good properties, as regards to the transit frequency ($F_t$). According to catalog, $F_t$ is equal up to 70 GHz. In practice a half of the transit frequency can be achieved, in our case it is max. 20 GHz.

4. Testing and Measurements

In the Fig.2 magnified view of the die of the realized structure is shown. All the input and output ports are highlighted. From the Fig.2 can be seen two grounds GND #1 and GND #2. It is because of the two power supply were used. Transmitter and receiver are powered separately due to independence on each other. This is also useful for testing structures under test, because we can directly say how much power will be enough for the each structure. All of input and output ports are matched to impedance of 50 Ω.

![Fig. 2. Magnified view of the realized monolithic structure.](image)

The power consumption of the transmitter is 0.835 W at the negative supply voltage -3.3 V and receiver 0.416 W at the same power supply voltage. The frequency range of the transmitter is from 200 MHz up to the recently tested value of 9 GHz (frequency of the external clock sine generator). This frequency range is dependent on the power of the clock signal. At the low frequencies (up to 500 MHz), a higher power approximately 0 dBm is needed. Stable operation at the higher frequencies (from 500 MHz up to 9 GHz) up to -7 dBm of the power level is guaranteed. Dimensions of this chip are 2 x 2 mm and will be encapsulated in the QFN32 package. The recently tested sample is only the silicon die. Testing process by using direct connect to the silicon wafer in the Fig.3 is illustrated. Micro-mechanical RF and DC test-
ing probes are shown. Testing with this instrument could not be too precise measuring method. There are several factors which must be taken into account, e.g. transient resistance or impedance matching. Nevertheless measurement results are sufficient to determine the functionality of the device under test.

Fig. 3. Testing of the monolithic structure by the direct connect to the silicon wafer.

Proper functionality and stability of the PRBS signal generator depend on the power of the signal from the clock generator has been tested. Clock generators that are generally used in case of UWB devices generate low power signals. In applications where a low-frequency sensing is needed, a more power for the stable functionality is necessary. If the PRBS generator is powered by the clock signal generator with output power is below 0 dBm up to the frequency 450 MHz, a proper functionality of the PRBS generator is not guaranteed. This dependence is shown in the Fig.4 below.

Fig. 4. Functionality dependence on the power of the clock signal

4.1. Generating of Stimulus Signals

The generator of the stimulus PRBS signal is a base part of the transmitter. Generated PRBS signal is a sequence of pseudo random generated bits. PRBS signal by the linear shift feedback register is generated. At the output of the PRBS generator is continuously generated sequence with parameters are equal to the true random signals. PRBS signals are periodic, therefore at the receiver side equivalent time sampling methods [7] can be applied. Length of the period depends on the order of the PRBS generator. Previous system used 8 or 12 bit linear shift register. Our SoC is powered by the 15 bit linear feedback register. More useful information about systems like this and base principles of generating PRBS signals in the article [8] can be found.

Sample of the generated PRBS signal in the time domain is shown in the Fig.5. Used frequency of the clock generator was 4 GHz. In the detailed section, generating of at least 4 bits of PRBS signal can be seen. This is not very smooth course and some jitter can be observed. It could be influenced by the several factors. Internal crosstalk directly in the monolithic structure, measurement error, because of 4 GHz is the maximal value of the used laboratory equipment or used measurement method as well.

Fig. 5. Generated MLBS sequence in the time domain.

4.2. Analog signal preprocessing

The main element of the wideband receiver is the track and hold (T&H) sampling block. Reasons to use sampling circuit in the receiver is to prepare the received signal, especially if it is a high-frequency signal with very high wide of the frequency band, which requires a very large sampling rate in order to take it back without any interference for example aliasing. Due to the very high wide of the frequency band of the transmitted stimulus PRBS signal proper conversion techniques to the digital form needs to be used. According to the generally known Shannon Kotelik’s theorem about the sampling of the signals, sampling frequency $F_s$ has to be two times higher than the maximum frequency of the signal to be processed. In our case, if we need to process the signal with frequency up to the maximum of the UWB band (approx. 12 GHz) use of the T&H sampling techniques will be the more effective solution. This solution is called equivalent time sampling [7]. At the output of the sampling gate, a preprocessed subsampled signal can be observed with the frequency suitable for the next A/D converting process.

T&H sampling gates are driven by the clock signal divided by the binary divider includes in the synchronization unit (see. Fig.1). According to the application of the UWB
radar, divider ratio by 64 or 128 can be used. The output signal from the sampling gate is shown in the Fig. 6. Hence, there is a reaction of the T&H amplifier to the clock signal can be observed. From the Fig. 6 two main operating modes of the sampling circuits can be seen. In the track mode, the signal is distributed from the input directly to the output of the receiver. If the hold mode is set, one sample of the processed signal is being grabbed for a short time slot. This is a periodic process controlled by the synchronization unit. At the hold event A/D converter takes one sample from the prepared sub-sampled signal. A/D converter is also powered by the same clock control signal as the T&H sampling gate. Subsampling method like this has a good performance in case of UWB radars, but strong synchronization between transmitter and receiver is needed. Also there are some deficiencies, e.g. jitter of the sampling circuits. For the proper functionality, good temperature conditions are necessary.

5. Conclusion

A brief overview of the differential fully integrated UWB radar realized as the structure on a single chip has been introduced. This process takes a lot of time and our effort to connect all of the building blocks into the integrated form. As a software tool, the modern studio called Cadence Virtuoso and his simulation modules and the newest version of libraries from the AMS were used. The main idea of this work was to make a testing monolithic structure to take a lot of information about this kind of integrated SoC. It was also very challenging and fruitful work to achieve desired results. Up to now, this structure is being tested for the proper stable function and stability in the meaning of internal oscillations. Finally, it can be interesting and challenging to realize a full scale UWB device, radar, also in the SoC form of one system in the package including a digital part as well. For this task, an another more powerful technology such as 0.25 µm SiGe mixed signal technology process can be a very interesting and suitable way. In this concept of the UWB radar, a new family of the transceiver and other circuit parts were used and tested, especially new PRBS generator. It leads to high resolution of this UWB radar, but in case of real-time processing will be the more difficult task for the computing unit. On the other side, offline signal processing with eight times better accuracy according to the previous version of UWB radar can be done. Therefore we can see much more for example around the comer.

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References


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